IN THE SPECIFICATION

Please amend the specification as shown below.

Replace the paragraphs beginning on page 3, lines 16-25 as follows:

In a first aspect, the present invention provides test circuitry for testing an integrated circuit, the integrated circuit being configurable to accept input data from stimulus scan cells and to provide output data to response scan cells, the test circuitry including: stimulus circuitry for providing test data to the integrated circuit; input selection means operable to control which of the test data and the input data are received at the integrated circuit; capture circuitry for capturing output data from the integrated circuit and generating response data; output selection means operable to select which of the output data and the response data are received by the response scan cells.

Replace the paragraphs beginning on page 4, lines 14-27 as follows:

In a particularly preferred embodiment, the test circuitry is configured for selective operation in a test mode and an operative mode, wherein: (a) in the test mode: the stimulus circuitry is configured to receive the input data from the stimulus scan cells; the input selection means is configured such that the integrated circuit receives the test data; and the output selection means is configured such that the response scan cells receive the response data; and (b) in the operative mode: the input selection means is configured such that the integrated circuit receives the input data; and the output selection means is configured such that the response scan cells receive the output data.

Replace the paragraphs beginning on page 5, lines 6-26 as follows:

Preferable, the stimulus circuitry includes: a dictionary storing a plurality of read/write operation primitives, the primitives being combinable to form at least a first read/write testing sequence; an address generator for generating addresses to which the primitives are written; and a librarian sub-block for receiving the input data, the input data being indicative of a test to be applied to the integrated circuit, the librarian sub-block being configured to control, on the basis of the input data, which of the primitives are provided to the integrated circuit, and the order in which they are provided, based on the input data.

In a second aspect, there is provided test circuitry for testing an integrated circuit, the test circuitry including stimulus circuitry and capture circuitry, the stimulus circuitry including: a dictionary storing a plurality of read/write operation primitives, the primitives being combinable to form at least a first read/write testing sequence; and a librarian sub-block for receiving the input data, the input data being indicative of a test to be applied to the integrated circuit, the librarian sub-block being configured to control, on the basis of the input data, which of the primitives are provided to the integrated circuit, and the order in which they are provided, based on the input data; wherein the capture circuitry captures response data from the integrated circuit.

Replace the paragraphs beginning on page 6, lines 5-20 as follows:

In a third aspect, there is provided a method of testing an integrated circuit using test circuitry associated therewith, the test circuitry including: stimulus circuitry; input selection means; capture circuitry; and output selection means; the integrated circuit being configurable to accept input data from stimulus scan cells and to provide output data to response scan cells, the method including the steps of: providing test data to the integrated circuit from the stimulus circuitry; operating the input selection means to control which of the test data and the input data are received at the integrated circuit; capturing output data from the integrated circuit using the capture circuitry; generating response data based on the output data; operating the output

selection means to select which of the output data and the response data are received by the response scan cells.

Replace the paragraphs beginning on page 7, lines 9-22 as follows:

In particularly preferred form, the test circuitry is configured for selective operation in a test mode and an operative mode, wherein: (a) in the test mode: the stimulus circuitry is configured to receive the input data from the stimulus scan cells; the input selection means is configured such that the integrated circuit receives the test data; and the output selection means is configured such that the response scan cells receive the response data; and (b) in the operative mode: the input selection means is configured such that the integrated circuit receives the input data; and the output selection means is configured such that the response scan cells receive the output data.

Replace the paragraphs beginning on page 7, line 28 through page 8, lines 1-23 as follows:

In a preferred form, the stimulus circuitry includes: a dictionary storing a plurality of read/write operation primitives, the primitives being combinable to form at least a first read/write testing sequence; an address generator for generating addresses to which the primitives are written; and a librarian sub-block for receiving the input data, the input data being indicative of a test to be applied to the integrated circuit, the librarian sub-block being configured to control, on the basis of the input data, which of the primitives are provided to the integrated circuit, and the order in which they are provided, based on the input data.

In a fourth aspect, the present invention provides a method for testing an integrated circuit using test circuitry, the test circuitry including stimulus circuitry and capture circuitry, the stimulus circuitry including: a dictionary storing a plurality of read/write operation primitives, the primitives being combinable to form at least a first read/write testing sequence; and a librarian sub-block; the method including the steps of: receiving input data at the librarian sub-

block, the input data being indicative of a test to be applied to the integrated circuit; selecting, on the basis of the input data and using the librarian sub-block, one or more of the primitives and an order of the primitives so selected; providing the selected primitives to the integrated circuit in the selected order; and capturing response data from the integrated circuit using the capture circuitry.